Research Statement

Ayse K. Coskun
Electrical and Computer Engineering (ECE) Department, Boston University (BU)

1 Overview

My research interests lie in the interface of electronic design automation (EDA), computing systems, and computer architecture. Specifically, my research focuses on improving the energy efficiency of computing systems through innovative techniques across the hardware-software stack.

Differentiating themes of my research in energy-efficient computing are: (1) developing application-aware, adaptive management techniques that consider dynamically changing user and environmental constraints, (2) providing cross-layer information flow among various hardware and software layers to enable better optimization, (3) considering the complex interplay among power, performance, and temperature, while most work in the area typically considers one or two of these parameters simultaneously, and (4) focusing on emerging interdisciplinary topics such as co-design of computing systems with novel cooling technologies or data center integration into smart grid programs.

The significance of my research contributions has been demonstrated in 1 book editorship, 2 book chapters, 10 accepted and published journal papers (4 additional journal papers are under review), 39 accepted and published proceedings papers in high-impact, refereed, top-notch conferences[1], 8 workshop papers, and 6 issued US patents. I have given over 45 invited talks (excluding conference paper presentations) since joining BU in September 2009. My research papers been cited for over 1000 times cumulatively[2], and my current *h-index* is **18**. I have received two *best paper awards*: at HPEC 2011 [W5] and VLSI-SoC 2009 [C28]. I am the recipient of the prestigious **2012 NSF CAREER Award**. Since September 2009, I have obtained **personal external funding of $1.14 million** from federal funding agencies, including NSF and Department of Energy Sandia National Laboratories, and industry, including Oracle, VMware, and AMD. I have also received the Richard Newton Graduate Scholarship (2011-12), which was given to only one junior faculty member every year at the Design Automation Conference (DAC).

This funding enabled me to establish and grow the Performance and Energy Aware Computing Laboratory (*PeacLab*) at Boston University. One of the most satisfying accomplishments was to see my first PhD student graduate in September 2013: Dr. Jie Meng has also received the best thesis award of the ECE Department and she is currently a software engineer in the high-performance computing (HPC) field at CGG Veritas in Houston, TX. Another one of my PhD students is on his way to graduate in Spring 2015. I am currently mentoring 6 PhD students at BU. I have also advised 9 Masters Projects during my time at BU, and hosted 4 undergraduate students, each student for multi-year research projects. All of the undergraduate students who were members of my lab co-authored technical conference papers with my PhD students and myself, and immediately started engineering careers in industry (at companies such as Akamai and BAE Systems) following their graduation. I currently host 3 undergraduate students and advise 2 Masters projects in my lab.

I have led multi-PI projects with collaborators from within BU and from external US and international universities such as at Brown University and EPFL, Switzerland. I strongly value close interactions with industry as I believe industry often brings a different perspective to research problems and pushes for high-impact, innovative, yet applicable solutions that can be implemented in real-life systems. I have found industry collaborations to be of high value to PhD students as well, as students have access to a larger set of experts and technologies through these collaborations. I have led funded collaborative projects with Oracle for 3 consecutive years, with VMware for 2.5 years, and with AMD for the last 2 years. I also have an on-going collaborative research project with IBM T.J. Watson Research Center.

In fact, evaluating the potential for *reduction to practice* and providing high-impact solutions to a broad community, which are often key elements in industry collaborations, are significant parts of most of my projects. For example, my students and I have contributed to the development of a 3D-stacked system prototype (Section 2.1) that demonstrated functional hardware and software together for the first time for a

[1] Conferences are the main publication venue in EDA (also in computer systems and architecture), and conference papers generally have higher impact than journal papers.
[2] According to Google Scholar: http://scholar.google.com/citations?user=euIQ_RkAAAAJ

3D multi-core processor; we have implemented majority of our proposed energy management techniques on real-life computing systems (Section 2.2); and we have developed and released simulators that enable temperature and energy estimations for novel architectures and systems (Sections 2.1 and 2.3). I have been also writing an invited bi-monthly column in the Circuit Cellar magazine, which has a world-wide circulation of over 20,000. My column articulates on how to implement green computing methods in practice for a broader engineering community.

I have been an active member of my research community (a detailed view on my academic service is available in my CV). Most significant duties include DATE Application Design Track Chair (current), DATE Green Computing Topic Chair/Co-chair (2012-14), VLSI-SoC Program Co-chair (2012), and technical program committee memberships at DAC and ICCAD, which are top-tier conferences in EDA. I have been selected as the GLSVLSI Program Chair for 2015 and General Co-chair for the same conference for 2016. As a result of the visibility of my research and my active service in the EDA community, I have been selected to serve as a member of the Executive Committee of the IEEE Council of EDA (CEDA) since January 2014. I have been a guest editor in ACM Transactions on Design Automation of Electronic Systems (TODAES) and currently serve as an associate editor for IEEE Embedded Systems Letters.

The following sections provide further details of my research on improving computing energy efficiency, organized by the research topic in a bottom-up fashion: designing better hardware nodes (2.1.), better node management policies (2.1.-2.2), and better data center level cost management policies (2.3-2.4).

2 Research Directions

2.1 Design and Management of 3D-Stacked Systems for Enabling Low-Power High-Performance Computing

Funding: NSF (CAREER), DAC Richard Newton Scholarship, Sandia National Laboratories, AMD
Collaborators: Y. Leblebici at EPFL, D. Atizenza at EFPL, AMD, IBM Zurich, A. Joshi at BU

My research on 3D-stacked systems has the goal to dramatically improve energy efficiency through leveraging (a) high-bandwidth, low-latency access among processor components on different layers in the stack, (b) integration of heterogeneous technologies in a single system (e.g., processors with DRAM or Silicon chips with optical layers), (c) flexible sharing of the computing resources among the layer owing to much shorter access delays compared to traditional design, and (d) integration with novel cooling technologies to provide dramatically higher throughput per volume and per watt.

My lab's research in 3D-stacked systems first addressed the modeling challenge as an essential step to the study of technology that is not currently available commercially. We designed a full-system simulation methodology, including transient performance, power, and temperature estimations in our DAC'12 and DATE'12 papers [C14,C16]. The simulation methodology required advancement of the performance and thermal simulators with capabilities that mimic 3D multi-core systems with on-chip DRAM. We released the thermal modeling method as part of the widely-used HotSpot simulator, and it has already been used by many academic researchers and also in industry by companies such as AMD. The modeling framework has enabled us to design adaptive management techniques that recognize application characteristics automatically and maximize throughput under power and thermal constraints [C14,J2].

We have also investigated the use of 3D stacking for designing many-core systems using a modular architecture that stacks the same multi-core layer multiple times, and demonstrated a functional *prototype* system at DATE'13 [C11]. This prototype was the first academic prototype that had a multi-core 3D design along with custom-designed software applications running on the system. Our analysis on the prototype led to the observation that by "pooling" the memory resources across different layers in a stack, it is possible to significantly improve performance. We have expanded this idea, and designed a "flexible heterogeneous" 3D system, which is homogeneous by design but can alter the memory resources allocated per core depending on application needs based on runtime application analysis [C6, J2].

Among the most significant challenges in designing high-performance 3D systems is the high temperature caused by the high-power density and the difficulty of cooling. We have demonstrated, in a highly-selective IEEE Micro Special Issue, that designing high-performance many-core "big chips" using 3D stacking and microchannel-based liquid cooling in between the stacks successfully eliminates thermal hot spots and pushes the achievable performance bounds [J11]. Our work published in IEEE Transactions on CAD on 3D

stacked systems with liquid cooling also optimized the cooling control [J10] and the microchannel design [J8], achieving between 20-50% additional reduction in system-level energy consumption and reducing the overall cooling requirement to only a few watts per layer for high-power many-core chips.

Recently, we have started investigating other heterogeneous integration scenarios for improving computing efficiency, such as using 3D stacking for integrating many-core systems with Silicon-photonics. We first demonstrated the thermal sensitivity of optical devices to temperature in DATE'14 [C2]. Our work synthesized the necessary knowledge from the circuits and devices domains, and presented a design-flow to optimize performance of many-core systems with optical networks. Our most recent work in this area starts to explore EDA problems for temperature- and power-aware placement of laser sources and optical devices [C1].

Our research in 3D system design and management has gained significant visibility, which is demonstrated by the high number of citations (despite most papers being published in the last few years), our 2 best paper awards [W5,C28], and 16 invited talks on this topic in addition to the high-quality research papers we have published. **Key differentiating factors** in our 3D systems research are: realistic evaluation of runtime behavior through detailed models as opposed to coarser-grained analysis that have been used in research prior to ours, exploring integration with novel technologies (such as liquid cooling and optical device layers), and adaptive management of the processor resources to maximize the potential of the 3D systems.

2.2 Managing Server Energy Efficiency

Funding: VMware, Oracle, Decision Detective Corp. (DOE SBIR subcontract)
Collaborators: Oracle, S. Reda at Brown University, J. Ayala at Complutense U. of Madrid

The diversity of the elements contributing to computing energy efficiency, i.e., CPUs, memories, cooling units, software application properties, availability of operating system controls and virtualization, etc., require system-level assessment and optimization. For this purpose, my work on managing server energy efficiency focuses on designing several key aspects: (1) necessary sensing and actuation mechanisms such that a server node can operate at a desired dynamic power level (i.e., power capping), (2) resource management techniques on native (not virtualized) and virtualized systems such that several software applications can efficiently share available resources, (3) cooling control mechanisms that are aware of the inter-dependence of performance, power, temperature-dependent portion of the power consumption (leakage), and cooling power.

The power capping technique we designed, *Pack & Cap*, leverages low-cost machine learning techniques to understand application behavior, and maximizes performance while closely tracking a dynamic power cap using *thread packing* in conjunction with voltage and frequency scaling. Our ICCAD'11 and MICRO'11 papers demonstrate the implementation of our technique on real-life servers [C19, C20]. We have also improved Pack & Cap with a feedback-controller in a highly-selective IEEE Micro Special issue [J9].

As many servers in data centers are virtualized and often multiple applications or virtual machines (VMs) run on the same server, resource sharing directly impacts performance and power. In our efficient server consolidation project with VMware, we have designed the necessary instrumentation and analysis techniques to estimate application demands, and leveraged this telemetry to optimize resource sharing [C9, C18]. Our new technique, vCap, which appeared at ISLPED'13, combines intelligent resource management with power capping, demonstrates the use of novel control knobs within the hypervisor for power management, and achieves 12% higher throughput compared to existing techniques while tracking a dynamic cap [C7].

Observing that most commercial servers are over-cooled and thus, are wasting energy, we designed efficient cooling control techniques for servers. Letting servers and data centers run hotter is already gaining attention in industry for reducing the cooling energy; however, the novel contribution of our work at DATE'13 is that our technique finds the optimum control setting considering the tradeoffs between temperature-dependent leakage power and the cooling power [C12]. In our lab, we experimentally demonstrated that our technique reduces server energy with no impact on performance on Oracle servers.

Distinguishing features of our work in this area are the use of learning mechanisms for automated characterization of application performance and power, implementation of all the developed techniques on real-life servers, and considering the non-trivial interactions among various physical phenomena (e.g., temperature vs. leakage) and various layers of hardware and software (e.g., control and telemetry mechanisms of applications, operating systems, and hypervisors).

2.3 Performance and Energy Management in HPC Data Centers

Funding: Sandia National Laboratories, MA Green High Performance Computing Center (MGHPCC)
Collaborators: Sandia Labs, M. Herbordt at BU, G. Schirner at Northeastern University

Additional levels of management and planning decisions take place at the data center level, and these decisions, such as job allocation across the computing nodes, impact energy consumption and performance. Our work in this domain jointly addresses optimizing the cooling energy of the data center and the performance of applications simultaneously for the first time for HPC data centers. HPC applications, such as the scientific computing loads running on Department of Energy machines, typically occupy many server nodes, run for a long time, and include heavy data exchange and communication among the threads of the application. For this reason, we optimized the job allocation by both minimizing the communication overheads among the nodes given to an application and selecting cooling-efficient nodes by modeling the heterogeneous heat circulation characteristics in a data center [C8, J5, J3].

This work has produced several key outcomes: First, we designed a simulation methodology to enable experimenting with various job allocation policies under realistic data center configuration and workload assumptions. Recently, we integrated this simulation methodology into Sandia Lab's Structural Simulation Toolkit (SST), which is a publicly available large-scale system simulator [J3]. Experimentation opportunities with large-scale real-life systems is rather limited in the community, thus, I expect this simulator to be of value to a number of researchers. Second, our novel joint optimization of communication-related overhead and cooling energy resulted in up to 50% reduction in cooling energy, while maintaining similar performance levels as existing performance-aware job allocation methods [C8, J3].

Our collaborative work with Sandia Labs also included designing tools to assess temperature-dependent reliability of servers and clusters in conjunction with multi-scale performance simulators [C13, C15].

2.4 Reducing Data Center Electricity Cost through Smart Grid Integration

Funding: Oracle, Decision Detective Corp. (DOE SBIR Subcontract)
Collaborators: M. Caramanis & Y. Paschalidis at BU, S. Reda at Brown University

How we are assessing *electricity cost* is changing following the developments in the smart grid and power markets. Instead of solely reducing the energy consumption of a data center, participation in *demand response* programs where the data center consumes power at levels as requested by the electricity provider may achieve lower overall cost. This is because providers are offering incentives for participation in such programs as they have to match supply and demand in real-time.

Our work in integrating data centers into the smart grid is the first to use data center as a grid load stabilizer [C3, C4, C5]. Specifically, we have focused on designing the necessary techniques to enable a data center to accurately follow a dynamic *regulation signal* broadcast by the provider. We designed the necessary optimization mechanisms that compute the power consumption to maintain a desired quality-of-service and also the regulation reserve amount the data center can offer in ICCAD'13 and CDC'13 [C4, C5]. In an invited special session at ASPDAC'14, we have demonstrated a policy that governs the number of active, idle, and sleeping servers along with the power level of each server so as to provide power tracking capabilities at every few second interval while maximizing the quality-of-service of the applications running in the data center.

Our work in this area, despite being very new, has gained immediate visibility, and resulted in invited talks and visits at several research institutions including Lawrence Berkeley National Labs (LBL) and Caltech and also in an invitation to for me to participate in the Energy Efficient High Performance Computing Working Group lead by LBL.

Uniqueness and strength of our work in this area are related to the synthesis of expertise on computing system power management, power markets/grid, and optimization theory. Unlike most of the existing work in the data center level optimization space and in data center-grid interactions, our experiments and proposed techniques are fully based on measurements and analysis on real-life computing systems. As a result, we can leverage the capabilities and limitations of servers and data center level management policies in our optimization scheme. Our ASPDAC'14 paper demonstrates up to 50% reduction in electricity cost in data centers when the data center participates in the regulation service reserves by running our control and optimization techniques.

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